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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/517,327	12/09/2004	Roland Brandl	AT02 0034 US	2949

65913 7590 03/20/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

NOTIFICATION DATE	DELIVERY MODE
03/20/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/517,327	BRANDL, ROLAND	
	Examiner	Art Unit	
	DHARTI H. PATEL	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Rao et al., Patent No. 5,770,886.

With respect to claim 1, applicant's acknowledged prior art [Fig. 1] teaches a data carrier [Fig. 1, 1] that includes an integrated circuit [Fig. 1, 5] which comprises a first terminal and a second terminal [Fig. 1, 6, 7], wherein the two terminals are provided for connection with transmission means [Fig. 1, 2] of the data carrier and an ESD protection circuit [Fig. 1, 8], which is connected between the two terminals [Fig. 1, 6, 7] and which comprises a series connection [Fig. 1, 9] consisting of a first protection diode [Fig. 1, 10] and a protection stage [Fig. 1, 11], which protection stage may be brought from a blocking state into a conductive state by exceeding a voltage threshold, and which comprises a second protection diode [Fig. 1, 12] connected in parallel with the series connection and in opposition to the first protection diode [Fig. 1, 10] of the series connection, and a rectifier circuit [Fig. 1, 13], which is connected to the ESD protection circuit [Fig. 1, 8] and comprises a rectifier diode [Fig. 1, 14] connected in parallel with the ESD protection circuit as disclosed in Specifications, Page 4, lines 9-18, 24-27, 32-33 and Fig. 1.

However, the prior art fails to teach or suggest that a rectifier diode of the rectifier circuit takes the form of a Schottky diode with a parasitic p/n junction and wherein the Schottky diode with the parasitic p/n junction forms a second protection diode of the ESD protection circuit.

Rao discloses an ESD protection circuit. Rao discloses an ESD protection circuit [Fig. 6, 101] and a rectifier diode [Fig. 6; 11], which takes the form of a Schottky diode with a parasitic p/n junction [Fig. 6; the Schottky diode 11 inherently consists of pure Schottky diode and a parasitic pn junction; as shown per applicant's own Fig. 3] simultaneously forms the second protection diode of the ESD protection circuit [Fig. 6, the Schottky diode 11 simultaneously forms the rectifier diode (the pure Schottky diode of Schottky diode 11) and the second protection diode (the parasitic p/n junction of Schottky diode 11), since it is inherent that the Schottky diode consists of pure Schottky diode and a parasitic pn junction; Schottky diode 11 turns on when there is excessive amount of current flowing in the reverse direction, and protects the circuit elements] connected between a power supply [Fig. 6, 15] and a ground [Fig. 6; col. 8; lines 8-12].

Both teachings are analogous electrostatic discharge protection circuits. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Rao's Schottky diode which is in parallel with ESD protection circuit as a second protection diode of the ESD protection circuit, with the integrated circuit for a data carrier of the applicant's acknowledged prior art because any abnormal reverse voltage applied to the LED system turns on the Schottky diode and diverts a large

portion of any abnormal reverse current away via the Schottky diode. Schottky diodes are well known for their ability to handle large reverse currents with negative effects.

With respect to claim 2, the acknowledged prior art teaches that the rectifier circuit [Fig. 1, 13] takes the form of a voltage doubler circuit [Specifications, Page 4, line 34].

With respect to claim 3, applicant's acknowledged prior art [Fig. 1] teaches a data carrier [Fig. 1, 1] for contactless communication with a communications stations, which data carrier comprises transmission means [Fig. 1, 2, Specification, Page 4, lines 1-6] and an integrated circuit [Fig. 1, 5] connected with the transmission means, which integrated circuit comprises a first terminal and a second terminal [Fig. 1, 6, 7], wherein the two terminals are provided for connection with transmission means [Fig. 1, 2] of the data carrier and an ESD protection circuit [Fig. 1, 8], which is connected between the two terminals [Fig. 1, 6, 7] and which comprises a series connection [Fig. 1, 9] consisting of a first protection diode [Fig. 1, 10] and a protection stage [Fig. 1, 11], which protection stage may be brought from a blocking state into a conductive state by exceeding a voltage threshold, and which comprises a second protection diode [Fig. 1, 12] connected in parallel with the series connection and in opposition to the first protection diode [Fig. 1, 10] of the series connection, and a rectifier circuit [Fig. 1, 13], which is connected to the ESD protection circuit [Fig. 1, 8] and comprises a rectifier diode [Fig. 1, 14] connected in parallel with the ESD protection circuit as disclosed in Specifications, Page 4, lines 9-18, 24-27, 32-33 and Fig. 1. Claim 3 differs from claim 1

by having a data carrier for contactless communication with a communications station. The teachings of Rao would apply to reject claim 3.

With respect to claim 4, the acknowledged prior art [Fig. 1] teaches that the rectifier circuit [Fig. 1, 13] takes the form of a voltage doubler circuit [Specifications, Page 4, line 34].

Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Rao et al., Patent No. 5,770,886, as applied to claims above, and further in view of Saitoh et al., Patent No. 6,570,490.

With respect to claims 7 and 9, the prior art discloses a rectifier circuit, but does not disclose that the rectifier circuit further comprises a second rectifier diode that takes the form of a Schottky diode.

Saitoh discloses an integrated circuit comprising a rectifier circuit [Fig. 4], which further comprises a second rectifier diode [Fig. 4, 73] that takes the form of a Schottky diode [Fig. 4, Schottky diode 73].

All three teachings are analogous integrated circuits connected between the power supply terminal and ground terminal. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Saitoh's rectifier circuit, into AAPA as modified by Rao, for the benefit of providing detection and rectification, and for power recovery [Saitoh; col. 1 lines 48-50, and 52].

With respect to claims 8 and 10, Saitoh discloses a rectifier circuit [Fig. 4] that further comprises a third rectifier diode [Fig. 4, 72] that takes the form of a Schottky

diode, but does not disclose a fourth rectifier diode. However, AAPA discloses a fourth rectifier diode [Fig. 1, 18]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a rectifier diode that takes the form of a Schottky diode in the rectifier circuit, for the benefit of providing more detection and rectification for the integrated circuit.

Response to Arguments

Applicant's arguments filed 12/21/2007 have been fully considered but they are not persuasive.

Applicant comments on page 5 of the REMARKS regarding claim 1 that the combination of AAPA in view of Rao does not teach or suggest a Schottky diode that simultaneously forms the rectifier diode and the second protection diode as recited in the amended claim 1.

The Examiner points out that the Schottky diode 11 of Rao simultaneously forms the rectifier diode (the pure Schottky diode of Schottky diode 11) and the second protection diode (the parasitic p/n junction of Schottky diode 11), since it is inherent that the Schottky diode consists of pure Schottky diode and a parasitic pn junction.

Applicant comments on page 5 of the REMARKS regarding claim 1 that using a Schottky diode to simultaneously form the rectifier diode and the second protection diode enables one diode with a p/n junction to be omitted from the integrated circuit. The Examiner points out that Rao's semiconductor device Fig. 6 utilizes only one Schottky diode 11, which simultaneously forms the second protection diode of the ESD

protection circuit and the rectifier diode. Fig. 6 of Rao does not include a regular diode with a p/n junction.

With respect to claim to the new claims 7-10, a new reference by Saitoh et al. [Patent No. 6,570,490] has been introduced to meet the limitations of rectifier circuit comprising second, third, and fourth rectifier diodes taking the form of a Schottky diode.

Based on examiner's best understanding, it is believed that the prior art references by the AAPA and Rao read on the amended claim language of independent claims 1 and 3. Accordingly, the rejections are maintained.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DHARTI H. PATEL whose telephone number is (571)272-8659. The examiner can normally be reached on 7:00 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Michael J Sherry/
Supervisory Patent Examiner, Art Unit 2836
/Dharti H Patel/
Examiner, Art Unit 2836
03/11/2008